DETAILED ACTION

Response to Arguments

1. Previous claim rejections under 35 U.S.C. 112 have been rendered moot in view of claim amendments as set forth below.

2. **Claim(s) 1-10** have been cancelled by the applicant.

EXAMINER'S AMENDMENT

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Patrick L. Miller on June 23, 2009.

The application has been amended as follows:

4. **Claim(s) 11-17** have been cancelled by an examiner's amendment.

5. **Claim 20 (currently amended)** The semiconductor integrated circuit device according to claim [[16]] 18, wherein the second voltage and the fourth voltage are the same.

Allowable Subject Matter

6. **Claim 18** is allowed.

7. The following is an examiner's statement of reasons for allowance: the pertinent prior art of record does not teach or suggest, in combination with the rest of the claim limitations, a semiconductor integrated circuit device comprising: " wherein a voltage

supplied to the plurality of bit lines pairs varies between a first voltage and a second voltage lower than the first voltage, wherein a voltage supplied to the plurality of search line pairs varies between a third voltage and a fourth voltage lower than the third voltage, wherein the first voltage is larger than the third voltage."

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. **Claim(s) 19 and 20** depend on independent claim 19 and is therefore allowed for at least the same reasons.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FERNANDO N. HIDALGO whose telephone number is (571)270-3306. The examiner can normally be reached on Monday-Friday, 7:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando N. Hidalgo/
Examiner, Art Unit 2827

/Hoai V. Ho/
Primary Examiner, Art Unit 2827